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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,851	08/06/2003	Jun Kanamori	MAE 292	7005

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,851	KANAMORI, JUN	
	Examiner	**Art Unit**	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Gurley

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 8/06/03. Currently, claims 1-19 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 8/06/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The disclosure is objected to because of the following informalities: page 8, lines 16-18, the examiner requests clarification with regards to, as stated, "The sidewalls 118 of the third embodiment can also be formed when the pad oxide film 108 is absent as in the second embodiment." According to the figures 2A-2B, the nitride film is absent in the second embodiment (figures 2A-2B). Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-14, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. US Patent 6,258,694 in view of Prabhakar US Patent 5,869,359.

Wang shows the semiconductor method substantially as claimed. See figures 1A-1F, and corresponding text, pertaining to claims 1 and 8, where Wang shows a method of fabricating a

semiconductor device, the method comprising: forming a first oxidation-resistant film **104** on the silicon layer (figure 1A; silicon substrate **100**); selectively removing the first oxidation-resistant film from parts of the silicon substrate (col. 2, lines 22-34); implanting oxygen ions **114** into selected parts of the silicon substrate, using the remaining parts of the first oxidation-resistant film as a mask (figure 1E; col. 2, lines 22-28 and lines 61-67; col. 3, lines 1-5); and oxidizing the selected parts of the silicon substrate (figure 1F; col. 2, lines 61-67; col. 3, lines 15-20), into which the oxygen ions have been implanted, to form isolation regions **202**, dividing the silicon substrate into a plurality of mutually isolated active regions (col. 1, lines 21-24; It is both inherent and well known that these techniques are used for isolation between devices). In addition, Wang shows, pertaining to claims 4 and 11, the method wherein the isolation regions are field oxide regions (col. 3, lines 15-20). Wang also shows, pertaining to claims 5, 6, 12 and 13, the method wherein the implanted oxygen ions have a concentration that varies from an upper surface of the silicon substrate to a lower surface of the silicon substrate and a peak concentration in a lower half of the silicon substrate (figure 1D and 1E; col. 2, lines 54-67; col. 3, lines 1-5 and lines 10-14, shows a higher concentration of oxygen being implanted; It is both inherent and well known that the implanted oxygen ions would have a concentration that varies from an upper and lower surface of the silicon substrate and a concentration in a lower half of the silicon substrate, since silicon conventionally includes an oxygen concentration at room temperature of 2.5 x $10^{15}/cm^3$. As a result, any additional oxygen ion implantation, within a specific region changes the concentration of the upper and lower surfaces of the substrate. See *Stanley Wolf and Richard N. Tauber,* *Silicon Processing For The VLSI Era,* *Vol. I, Second Edition, page 19, under 1.3.51 Oxygen and Carbon Measurements in Silicon Using Infrared*

Absorbance Spectroscopy). Wang shows, pertaining to claims 14, 16, and 17, the method further comprising forming an oxide film **102** (figure 1A) on the silicon substrate, the first oxidation-resistant film being formed on the oxide film, wherein the first oxidation-resistant film **104** comprises at least one of a nitride film and a photoresist film, and further comprising selectively removing the oxide film before the oxygen ions are implanted (col. 2, lines 22-33, nitride layer; It is well known process to form the same, i.e. photoresist and lithography). Finally, Wang shows, pertaining to claims 18 and 19, the method further comprising: depositing a second oxidation-resistant film **110** after the first oxidation-resistant film has been removed from the parts of the silicon substrate (figure 1C; col. 2, lines 44-53); and etching the second oxidation-resistant film to leave sidewalls on vertical edges of the remaining parts of the first oxidation-resistant film before the oxygen ions are implanted (col. 2, lines 44-53), wherein the second oxidation-resistant film is an oxide film or a nitride film (col. 2, lines 47-49, nitride layer).

However, Wang fails to show, pertaining to claims 1-19, a method of fabricating a semiconductor device, having a silicon layer disposed on an insulating film where oxygen ions are implanted into the selective parts of the silicon layer and oxidized to form field oxide regions. In addition, Wang fails to show, pertaining to claims 2 and 9, the silicon layer having a thickness of at most seventy nanometers. Wang also fails to show, pertaining to claims 3 and 10, the method wherein the semiconductor device is a fully depleted silicon-on-insulator device.

Prabhakar teaches in figures 1-10, and corresponding text, a semiconductor device, including field oxide regions formed within a silicon layer, pertaining to claims 1-19, a method of fabricating a semiconductor device, having a silicon layer (silicon on insulator (SOI)). Prabhakar also teaches, pertaining to claims 2 and 9, that the silicon layer has a thickness of at

most seventy nanometers. Finally, Prabhakar teaches, pertaining to claims 3 and 10, the method wherein the semiconductor device is a fully depleted silicon-on-insulator device.

It would have been obvious to one of ordinary skill in the art to have incorporated, substituting the silicon substrate with the SOI substrate, implanting oxygen ions into selected parts of the silicon layer (with a thickness of at most seventy nanometers), and oxidizing the selected parts to form field oxide regions within the silicon layer where the completed device is a fully depleted SOI device, in the method of Wang, pertaining to claims 1-19, according to the teachings of Prabhakar, with the motivation that, as stated in col. 1, lines 15-27; col. 4, lines 27-57, the fully depleted SOI device taught by Prabhakar, includes the use of field oxide regions formed within the selected parts of the silicon layer, where conventional technology teaches that these regions are used for the purpose of device isolation. In addition, one of ordinary skill in the art would be drawn to use of a thin SOI layer, taught in Prabhakar, with the motivation that, the SOI substrate produces lower parasitic capacitances for greater channel current, which in turns allows for faster switching speed.

Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang US Patent 6,258,694 in view of Prabhakar US Patent 5,869,359 in further view of Ishii et al. US Patent 6,596,593.

Wang in view of Prabhakar shows the semiconductor method substantially as claimed, including a silicon layer disposed on an insulating film. See the previous 35 U.S.C. 103(a) rejection, pertaining to claims 1-19.

However, Wang in view of Prabhakar fails to show, pertaining to claims 7 and 15, the method wherein implanting oxygen ions comprises: forming an oxide film on the silicon layer; and implanting the oxygen ions through the oxide film into the silicon layer.

Ishii teaches in figures 1-14, and corresponding text, a semiconductor device, that includes field oxide regions, pertaining to claims 7 and 15, wherein an oxide film is form on the semiconductor substrate and oxygen ions are implanted through the oxide film to form isolation regions within the substrate (figures 12 and 13; col. 8, lines 7-9 and lines 32-52).

It would have been obvious to one of ordinary skill in the art to have incorporated, implanting oxygen ions through the oxide film into the silicon layer, in the method of Wang in view of Prabhakar, pertaining to claims 7 and 15, according to the teachings of Ishii, with the motivation that, as stated in Ishii, col. 8, lines 7-9 and lines 32-52, the oxygen ion implantation process through the oxide film and the annealing process are used for the purpose of creating a reliable isolation region **111** within the semiconductor substrate, which is compatible with the method of Wang in view of Prabhakar, wherein it is both well both known and conventional that these regions are used for the purpose of device isolation between semiconductor devices. Additionally, it is well known that implantation through the oxide will help prevent damage to the crystalline structure of the underlying layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
August 12, 2004

Lynne A. Gurley

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